REMARKS

The Office Action mailed April 19, 2004, has been received and reviewed. Claims 6, 7, and 17-22 are currently pending in the application. Claims 6, 7, and 17-22 stand rejected. Applicants have amended claims 6, 7, 17, and 20-22, canceled claim 19, added new dependent claims 23-27, and respectfully request reconsideration of the application as amended herein.

35 U.S.C. § 112 Claim Rejections

Claims 19-22 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicants have canceled claim 19 and have amended claims 20-22 to depend from independent claim 6, rendering the objection moot.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 4,782,037 to Tomozawa *et al.* and U.S. Patent No. 5,428,244 to Segawa *et al.*

Claims 6 and 7 stand rejected under 35 U.S.C. § 103(a) ("Section 103") as being unpatentable over U.S. Patent No. 4,782,037 to Tomozawa *et al.* ("Tomozawa") and U.S. Patent No. 5,428,244 to Segawa *et al.* ("Segawa"). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103 rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The obviousness rejection of claims 6 and 7 is improper because the cited references do not teach or suggest all the limitations of the claimed invention and do not provide a motivation to combine to produce the claimed invention.

Tomozawa discloses a process of fabricating a semiconductor integrated circuit device to prevent a refractory metal layer from peeling off the semiconductor integrated circuit device. To form the semiconductor integrated circuit device, an insulating film is formed on a semiconductor substrate. A conductive layer formed from polycrystalline silicon is deposited over the insulating film. A refractory metal layer, such as a refractory metal silicide layer, is formed over the conductive layer. Another insulating film is then formed over the refractory metal layer. This insulating film is a layer of silicon dioxide formed by chemical vapor deposition at a temperature of 400°C or at a temperature of 700°C to 800°C. Alternatively, the insulating film is a layer of silicon nitride.

Segawa discloses a method of promoting adhesion between a metallic silicide film and an overlaying dielectric layer and for decreasing peeling during subsequent heat treatments. The method includes forming a metallic silicide layer and a silicon-rich dielectric cap during the formation of a gate stack structure. The silicon-rich dielectric cap has a silicon-to-other element (*e.g.*, oxygen or nitrogen) ratio that includes a silicon content that is higher than the silicon-to-other element ratio according to the stoichiometric composition of the formula of the deposited material. The silicon-rich dielectric cap is formed from silicon oxide or silicon nitride. The temperature used during the formation of the silicon-rich dielectric cap over the metallic silicide layer exceeds 600°C. In Examples I, II, V, and VI, a temperature of 840°C is used in forming the silicon-rich dielectric cap from silicon dioxide. In Examples III and IV, a temperature of 760°C is used in forming the silicon-rich dielectric cap from silicon nitride. In Example VII, a temperature range of 650°C to 700°C is used in forming the silicon-rich dielectric cap from silicon oxide. In Example VIII, a temperature range of 650°C to 700°C is used in forming the silicon-rich dielectric cap from silicon nitride.

As amended, claim 6 recites a method of forming a gate stack. The method comprises forming a gate dielectric layer on a silicon substrate and forming a polysilicon layer on top of the gate dielectric layer. The polysilicon layer is subjected to an ion implantation of impurities. A

metallic silicide film is deposited in a non-annealed state atop the polysilicon layer. A dielectric cap layer formed from silicon nitride is deposited over the metallic silicide film at a temperature below about 600°C. The temperature is sufficiently low to maintain the metallic silicide film in the non-annealed state.

The cited references do not teach or suggest the limitation of "depositing a dielectric cap layer formed from silicon nitride over the metallic silicide film at a temperature below about 600°C, wherein the temperature is sufficiently low to maintain the metallic silicide film in the non-annealed state," as recited in claim 6. While Tomozawa teaches that its insulating film is formed from silicon nitride, Tomozawa does not teach temperature conditions at which the insulating film is formed. Tomozawa only teaches temperature conditions at which a silicon dioxide insulating film is formed. Furthermore, as acknowledged by the Examiner, Segawa does not teach or suggest a method for forming a dielectric cap layer at a temperature below about 600°C and, therefore, necessarily does not teach that a dielectric cap layer formed from silicon nitride is formed at this temperature. See Final Office Action dated April 8, 2003, p. 4.

The cited references also do not teach or suggest the limitation of "depositing a metallic silicide film in a non-annealed state atop the polysilicon layer" as recited in claim 6. Neither Tomozawa nor Segawa teaches that their respective refractory metal layer or metallic silicide film is deposited in a non-annealed state.

The cited references also do not provide a motivation to combine to produce the claimed invention. The Examiner acknowledges that Tomozawa does not teach the limitation of "subjecting the polysilicon layer to an ion implantation of impurities" and, therefore, relies on Segawa as teaching this limitation. Office Action of April 19, 2004, p. 2. The Examiner states that "it would have been obvious for one skill [sic] in the art at the time of the invention to form the impurity in the polysilicon in light of Segawa because Segawa describes further step that is silent by Tomozawa in order to form impurity in the polysilicon with a reasonable expectation of success." *Id.*

To provide a motivation or suggestion to combine, the prior art or the knowledge of a person of ordinary skill in the art must "suggest the desirability of the combination" or provide "an objective reason to combine the teachings of the references." M.P.E.P. § 2143.01. Evidence

of the motivation to combine "must be based on objective evidence of record" and can not "be resolved on subjective belief and unknown authority." *In re Lee*, 61 U.S.P.Q.2d 1430, 277 F.3d 1338, 1343-1344 (Fed.Cir. 2002). The Examiner's proposed motivation to combine in this case is improper because it is conclusory and is not based on objective evidence of record. Contrary to the Examiner's assertions, nothing in Tomozawa or Segawa, when combined, provides any motivation to combine to produce the claimed invention. Specifically, nothing in Tomozawa provides any suggestion to implant impurities in its conductive layer by ion implantation. In addition, nothing in Segawa provides any suggestion to use ion implantation in the fabrication of other gate stack structures.

Furthermore, even assuming *arguendo* that the Examiner's proposed motivation to combine is proper, the cited references still do not teach or suggest all of the claim limitations, as discussed above.

Since the cited references do not teach or suggest all the limitations and do not provide a motivation to combine, the obviousness rejection of claim 6 is improper and should be withdrawn.

Claims 20-22 are allowable as depending from an allowable base claim.

Claims 20 and 21 are further allowable because the cited references do not teach or suggest that the dielectric cap layer is deposited at a temperature of between 400°C and 600°C, such as at 500°C.

Claim 22 is further allowable because the cited references do not teach or suggest that the dielectric cap layer is deposited on the metallic silicide film at a temperature sufficiently low to preclude formation of silicon clusters in the metallic silicide film.

As amended, claim 7 recites a method of forming a gate stack. The method comprises forming a gate dielectric layer on a silicon substrate and forming a polysilicon layer on top of the gate dielectric layer. The polysilicon layer is subjected to an ion implantation of impurities. A metallic silicide film is deposited in a non-annealed state atop the polysilicon layer. A dielectric cap layer formed from silicon nitride is deposited over the metallic silicide film at a temperature below about 600°C. The temperature is sufficiently low to preclude formation of silicon clusters in the metallic silicide film.

The cited references do not teach or suggest the limitations of "depositing a dielectric cap layer formed from silicon nitride over the metallic silicide film at a temperature below about 600°C, wherein the temperature is sufficiently low to preclude formation of silicon clusters in the metallic silicide film" and "depositing a metallic silicide film in a non-annealed state atop the polysilicon layer" for substantially the same reasons discussed above in the obviousness rejection of claim 6.

The cited references also do not provide a motivation to combine to produce the claimed invention for substantially the same reasons discussed above in the obviousness rejection of claim 6.

Claims 23 and 24 are allowable as depending from an allowable base claim.

Claims 23 and 24 are further allowable because the cited references do not teach or suggest that the dielectric cap layer is deposited at a temperature of between 400°C and 600°C, such as at 500°C.

Since the cited references do not teach or suggest all the limitations and do not provide a motivation to combine, the obviousness rejection of claim 7 is improper and should be withdrawn.

Obviousness Rejection Based on Tomozawa and Segawa and further in view of U.S. Patent No. 5,438,006 to Chang *et al.*

Claims 17 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tomozawa and Segawa, and further in view of U.S. Patent No. 5,438,006 to Chang *et al.* ("Chang"). Applicants respectfully traverse this rejection, as hereinafter set forth.

The obviousness rejection of claims 17 and 18 is improper because the cited references do not teach or suggest all the limitations of the claimed invention and do not provide a motivation to combine to produce the claimed invention.

The teachings of Tomozawa and Segawa are as previously described.

Chang discloses an integrated circuit device having a reduced height gate stack. The gate stack includes a patterned polysilicon layer and a patterned metal layer. Chang discloses that this is in contrast to a conventional gate stack, which also includes an overlying oxide layer. See

Column 3, lines 4-8. The gate stack is fabricated by forming a gate oxide layer and a field oxide layer on a silicon substrate. A polysilicon layer is formed over the oxide layers and a refractory metal layer is formed over the polysilicon layer. Chang discloses that the height of the gate stack is reduced by removing a silicon dioxide mask layer. The patterned metal layer is used as a mask to etch a polysilicon layer to form the patterned polysilicon layer.

As amended, claim 17 recites a method for forming a gate stack. The method comprises providing a semiconductor substrate with a dielectric layer on an active surface of the semiconductor substrate. A polysilicon layer is disposed over the dielectric layer and a metallic silicide film in a non-annealed state is formed over the polysilicon layer. A dielectric cap is formed from silicon nitride on the metallic silicide film at a sufficiently low temperature so that the metallic silicide film remains in the non-annealed state. A resist layer is formed and patterned on the dielectric cap. The dielectric cap, the metallic silicide film, and the polysilicon layer are etched and the resist layer is stripped.

The cited references do not teach or suggest the limitations of "forming a dielectric cap from silicon nitride on the metallic silicide film at a sufficiently low temperature so that the metallic silicide film remains in the non-annealed state" and "forming a metallic silicide film in a non-annealed state over the polysilicon layer."

Tomozawa and Segawa do not teach forming the dielectric cap from silicon nitride at a sufficiently low temperature so that the metallic silicide film remains in the non-annealed state. Rather, as previously discussed, Tomozawa teaches temperature conditions at which a silicon dioxide layer is formed and Segawa teaches a dielectric cap layer formed at high temperatures. Chang does not cure these deficiencies in Tomozawa and Segawa because Chang provides no teaching or suggestion of forming a dielectric cap layer on its refractory metal layer and, therefore, necessarily does not provide a temperature at which such a dielectric cap layer is deposited.

The cited references also do not teach or suggest that a metallic silicide film is formed in a non-annealed state over the polysilicon layer, as recited in claim 17. Tomozawa, Segawa, or Chang do not teach that their respective refractory metal layers or metallic silicide film are deposited in a non-annealed state.

The Examiner acknowledges that Tomozawa and Segawa do not teach the limitation of forming and patterning a resist layer on the dielectric cap and relies on Chang as teaching this limitation. The Examiner states that "[i]t would have been obvious for one skill [sic] in the art at the time of the invention in light of Chang to use a resist layer because as shown in Chang the resist is used as a mask in order to pattern and etch other layers including the insulating layer." *Id.* at p. 3. However, the Examiner's proposed motivation to combine is improper because it is conclusory and is not based on objective evidence of record. Nothing in Tomozawa, Segawa, or Chang, when combined, provides any motivation to combine to produce the claimed invention. Specifically, nothing in Tomozawa or Segawa provides any suggestion to form and pattern a resist layer on the dielectric cap. In addition, nothing in Chang provides any suggestion to form and pattern a resist layer on the dielectric cap during the fabrication of other gate stack structures.

Furthermore, even assuming *arguendo* that the Examiner's proposed motivation to combine is proper, the cited references still do not teach or suggest all of the claim limitations, as discussed above.

Since the cited references do not teach or suggest all the limitations and do not provide a motivation to combine, the obviousness rejection of claim 17 is improper and should be withdrawn.

Claim 18 is allowable as depending from an allowable base claim. Claim 18 is further allowable because the cited references do not teach forming the dielectric cap at a temperature below about 600°C.

New claims 25-27 are allowable as depending from an allowable base claim.

New claims 25 and 26 are further allowable because the cited references do not teach or suggest that the dielectric cap layer is deposited at a temperature of between 400°C and 600°C, such as at 500°C.

Claim 27 is further allowable because the cited references do not teach or suggest that the dielectric cap is deposited on the metallic silicide film at a temperature sufficiently low to preclude formation of silicon clusters in the metallic silicide film.

ENTRY OF AMENDMENTS

The amendments to claims 6, 7, 17, and 20-22 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add new matter to the application. Support for the amendments is found in the as-filed application at at least p. 6, lines 13-18, p. 6, lines 25-28, and p. 9, lines 1-6.

Support for new claims 23-27 is found in the as-filed application at at least p. 4, lines 15-17 and p. 9, lines 2-6.

CONCLUSION

Claims 6, 7, 17, 18, and 20-27 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

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